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# Methods for the Construction of Protection with Magnetosensitive Elements for the Parallel Circuits with Single end Supply

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***Abstract*—The conventional transverse protection for the parallel circuits is considered. Its disadvantages and the methods for their elimination are discussed. It is noted, that the present protection has been proposed based on monitoring the currents ratio in the phases of the same name, and devoid of all the disadvantages of the conventional one, except for its use of current transformers with ferromagnetic cores. It is stated that the protections without current transformers construction problem is a fundamentally unresolved problem of relay protection. Three ways to solve it for parallel lines are proposed. The first and the second are to do it at the power supply side, the third one - at the receiving side. The first is to determine the damaged line by the time difference of reaching the set value by the currents in the same name phases, the line in which the current has reached the set value earlier is disconnected; the second is to control the angle between the differential current of the parallel lines and the current in each of the same name phases, the third is to control the time between the moments when the current in the line phase reaches the specified value. The circuits where these methods are implemented, are analyzed. With the help of mental modeling, their performance in various modes is confirmed.**

***Keywords*—magnetosensitive element, method, protection, parallel power lines, mental modeling**

## I. Introduction

For the past hundred years, transverse differential current directional protection with the following disadvantages has been widely used for the 6-35 kV parallel lines protection: low sensitivity due to tuning out from currents in intact phases and maximum load currents, the presence of voltage and dead zone circuits, as well as receiving information from conventional current transformers with ferromagnetic cores. Several times over the last century, solutions were proposed that eliminated one or another disadvantage, for example, voltage circuits were excluded in [1], the dead zone in [2], and the correct protection behavior during wire breaks was ensured in [3, 4], also attempts were made to increase its sensitivity [5]. But finally, most of the disadvantages were eliminated only in recent years [6–10]. For example, in [7], due to the new principle of protection construction, namely controlling the current ratio in the same name phases, it was possible to ensure high sensitivity (cascade zone does not exceed 11% of the line length), exclude voltage circuits and ensure correct operation in all modes. However, one of the current transformers use disadvantages, which is inherent in the vast majority of power supply system elements relay protection devices, is inherent also in parallel line protections, including the latest protections, for example [11–13]. Avoiding the use of current transformers in recent decades is considered a fundamentally unresolved problem of relay protection, which was repeatedly mentioned at the CIGRE sessions [14, 15]. The fact is that current transformers are big and heavy, and produce errors in transient conditions. For example, a 10 kV current transformer, installed in complete switchgears, weighs 18 kg, of which 2 kg are high-quality copper and 10 kg are stainless steel, and their weight for complete current conductors can reach 500 kg. One way to solve this problem is to construct protections that receive the necessary information from magnetosensitive sensors. The principles of constructing maximum current [16–18], phase differential [19, 20], differential [21–23] and distance [24, 25] protections, as well as principles for detecting reverse and zero sequence currents [26], have already been developed on this base. In this paper, we consider methods for constructing protections with reed switches and inductors without using current transformers for parallel lines with one-sided power supply that are developed by the authors. Herewith, it was possible to eliminate almost all of the above disadvantages at the same time and quite simply. Reed switches and inductors are selected due to the fact that reed switches are widely used in engineering [27] and have some advantages that are important for RP [28], and inductors are small-sized, convenient, not affected by temperature, and have been successfully used for a long time in RP, specifically as current converters [16].

## II. Method for Protecting Parallel Lines at the Power Supply Side

### *A. The protection method based on the time difference in the given value achievement by currents of the specified values*

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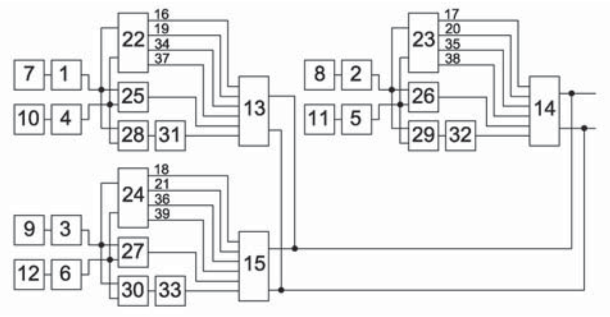


Fig. 1. Block diagram of the parallel lines protection from the supply side

The method [29] is to control the time $t_1$ between the moments when the instantaneous currents $i_1$ and $i_2$ in the same name phases reach the given (reference) value $i_{ref}$. If $t_1$ exceeds the setting $t_{ref1}$ of the protection trip, it turns off a line in which the current has reached a predetermined value earlier. We show the protection efficiency in various modes using mental modeling, which, as is known [30], is a kind of modeling and a logical analogy of real experience. In the load mode, the protection (Fig. 1) does not work, since the threshold values in units 1-6 fixing the current reaching the set value in the line phase, connected to the current sensors 7-12 are selected with large load currents. Therefore, there are no signals at the outputs of the logic units 13, 14, 15.

In case of short circuits (SC) on the buses of the opposite substation, the currents in the damaged phases of the lines are sufficient for the operation of units 1-6. Therefore, they produce signals. Moreover, due to the presence of various errors, the signals at the outputs of the current sensors installed under the same name phases reach the threshold value at different times. For example, if units 4, 5, 6 were the first to operate, then signals appear at the outputs 16, 17, 18 and 19, 20, 21 of units 22, 23, 24 determining the sequence of units 1-6 trips and at the inputs of time $t_1$. measurement units 25, 26, 27. After the operation of units 1, 2, 3, the signals at the outputs 16, 17, 18 are saved, and disappear at the outputs 19, 20, 21. The units 25, 26, 27 and the units 28, 29, 30 for time recording which takes the current in the same name phases of the lines to exceed the specified value. The latter start the time delay units 31, 32, 33 $t_2$ ($t_2$ is necessary to ensure the protection correct operation in cascade short-circuit trip modes). As a result, the logic units 13, 14, 15 receive signals from units 22, 23, 24 about which of units 1 and 2, or 3 and 4, or 5 and 6 worked first, from units 25, 26, 27 about the time value $t_1$, and from units 31, 32, 33 about the time lapse $t_2$. The units 13, 14, 15 do not give a signal, since the time $t_1$ does not exceed the set value $t_{ref1}$ and there are no signals at any of the outputs 34 or 19, 35 or 20, 36 or 21 of units 22, 23, 24 due to the fact that units 1-6 trip or don't trip if the short circuit is eliminated. The protection does not work.

With a three-phase short circuit in one of the lines, for example, in the first one, the currents in its phases exceed the currents in the same name phases of the second line.

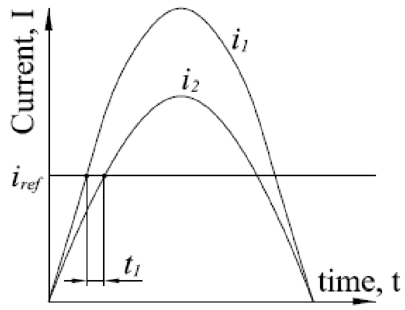


Fig. 2. The time between the moments when the currents $i_1$ and $i_2$ reach the set value $i_{ref}$

Therefore, units 1, 2 and 3 trip before units 4, 5 and 6, and signals appear at outputs 34, 35, 36 and 37, 38, 39 of units 22, 23, 24. After the units 4, 5 and 6 trip, signals appear at the outputs of units 25, 26, 27. The time $t_1$ (Fig. 2) exceeds $t_{ref1}$, and the units 13, 14, 15 trip, giving a signal to disconnect the first line. Similar method is used to analyze other modes of protection work.

### *B. A device for protecting four parallel lines implementing the proposed method using reed switches*

Based on the method of parallel lines protection at the supply side, a circuit [31] for protecting four parallel lines was developed, where reed switches 1-12 are used as current sensors (Fig. 3) installed at a safe distance from the conductor buses of phases A, B, C of the first , second, third and fourth lines. The proposed device also contains: OR elements 13, 14, 15, 16, AND elements 17 with one inverse input, OR-NOT elements 18, 20, AND elements 19, 21, identical units 22, 23 and 24 for determining a line damage. For example, the damaged line determination unit 22 contains the MEMORY elements 25, 26, 27, 28, 37, 38, 39, 40, 49, 50, 51, 52, 58, AND elements 29, 30, 31, 32, 60, 61, 62, 63 with one inverse input, time relay 33, 34, 35, 36, 59, AND elements 41, 42, 43, 44, 54, OR elements 45, 46, 47, 48, 53, 55, 56, 57.

In load mode, currents in the line phases are insufficient for the operation of reed switches 1-12. Therefore, there are no signals at the damaged line detection units 22, 23, 24 and the elements OR 13, AND 17, 19, 21 outputs. The protection does not work. With a single-phase short circuit in one of the lines, for example, in phase A of the first one, the reed switches 1, 4, 7, 10 are triggered by the induction of a magnetic field created by a short circuit current, and the reed switches 2, 3, 5, 6, 8, 9, 11, 12 are triggered by a magnetic field created by currents in intact phases. Therefore, the inputs of the units 22, 23, 24 receive signals. In this case, the unit 22 is triggered, giving a signal to the input of the OR element 13, and the units 23 and 24 do not give signals, since the time between the reed switches 2, 5, 8 and 11 trips, as well as 3, 6, 9 and 12 does not exceed $t_{ref1}$. Consider the operation of block 22. Reed switch 1 is triggered earlier than reed switches 4, 7, 10, so the current in phase A of the first line is greater than the currents in the same name phases of the remaining lines, and gives a signal.

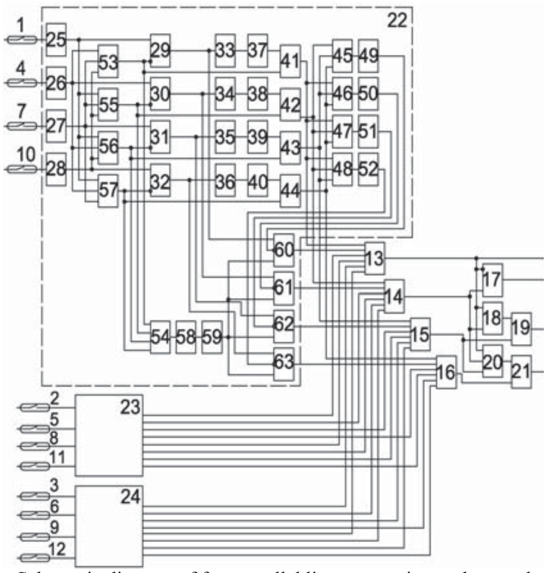

Fig. 3. Schematic diagram of four parallel lines protection at the supply side.

The MEMORY element 25 remembers the signal received from the reed switch 1, for example, for 0.01 s (eliminates the false protection trip by disconnecting the undamaged line when the contacts of the reed switches open), and sends it to the inputs of the OR elements 55, 56, 57 and the AND element 29, whose inverse input does not receive a signal from the OR element 53, since the reed switches 4, 7 or 10 have not yet tripped. The AND element 29 starts the time relay 33, and the OR elements 55, 56, 57 start the AND element 54 and block the operation of the AND elements 30, 31 32, therefore there are no signals at the outputs of the time relay 34, 35, 36, MEMORY 38, 39, 40, AND 42, 43, 44, 61, 62, 63 elements. Time relay 33 activates and sends a signal to the MEMORY element 37 input, since the time until the contacts of one of the reed switches 4, 7 or 10 are closed exceeds the set value $t_{ref1}$, tuned out from $t_{unb}$ ( $t_{unb}$ is the time between the reed switches trips arising due to the influence of errors caused by inaccuracies in installation, calculations, etc. with external three-phase SCs). The MEMORY element 37 records it, stores it for the duration of the protection, for example 0.1 s, and sends it to an input of the AND element 41. After the reed switches 4, 7 or 10 trip, the OR element 53 sends a signal to the inverse input of the AND element 29 and the inputs of the AND elements 41 and 54. Therefore, the time relay 33 is returned to its original state, and the elements AND 41, 54 send signals. From the output of the AND element 41, the signal goes to the inputs of the OR elements 46, 47, 48, through which it is fed to the inputs of the MEMORY elements 50, 51, 52 (they store the signal, for example, for 0.3 s, which enables to send the signal to the time relay 47, 48, 49 inputs until the protection on the opposite side is activated and the corresponding switch is turned off and until the proposed protection is activated, which ensures reliable protection operation when the damage is cascaded), and to the input of the OR element 13. The MEMORY elements 50, 51, 52 give a signal to the inverse input of the AND elements 61, 62, 63, blocking their operation. The OR element 13 gives a signal to disconnect the first line switch and blocks the operation of the elements AND 17, OR NOT 18, 20. When a single-phase short circuit occurs in phase B, only unit 23 trips, and in case of short circuit in phase C - unit 24. With a two-phase or three-phase short circuit, for example on the first line, two of the three units 22, 23, 24, trip, respectively, depending on what phases the short circuit is, or all three blocks 22, 23, 24, trigger the OR element 13 that sends a signal to disconnect the switch of the first line and blocks the operation of elements AND 17, OR NOT 18, 20. With a single-phase short circuit in the cascade zone, for example, in phase A of the first line, the reed switches 1, 4, 7, 10 trip. At the same time, the AND elements 41, 42, 43, 44 do not send signals, since the time between the reed switches trips does not exceed the specified value $t_{ref1}$, and the AND 54 and MEMORY 58 elements send signals, since the reed switches 1, 4, 7, 10 trip, and start the time relay 59. After the first line switch is disconnected on the opposite side, the reed switch 1 continues to operate, but the reed switches 4, 7, 10 do not, since the currents in the phases of the remaining lines decrease. At the same time, the AND element 60 sends a signal, since its direct inputs received signals from the AND element 29 and the time relay 59 (the exposure time $t_{ref2}$, for example 0.3 s, has elapsed, it is tuned out from the time necessary for the protection to trip on the opposite side and disconnect the corresponding switch), but the inverse input from the MEMORY element 49 did not. The OR element 13 trips and sends a signal to disconnect the first line.

With double earth faults, for example in phase A of the first line and in phase C of the second line, reed switches 1 and 6 trip earlier than reed switches 4, 7, 10 and 3, 9, 12, respectively, since the currents in the indicated phases of the lines exceed those in the same name phases. Therefore, unit 22 sends a signal to the input of the OR element 13, and unit 24 to the input of the OR element 14. In this case, the OR element 13 gives a signal to disconnect the switch of the first line and to the inverse input of the AND element 17, blocking the protection operation to disconnect the switch of the second line. Similarly, protection behavior in other modes is considered.

### *C. A protection method that controls the angle between the differential current of parallel lines and the current in each of the same name phases*

The method is to control: the same name line phases currents absolute values sum ratio to their difference, the presence of currents in the same name line phases, the difference between the angle $\varphi_1$ ( $\varphi_1$ is the phase angle between the current $\underline{I}_{i2}$ in the *i*-th phase of the second line and the resulting current obtained by subtracting the first current line $\underline{I}_{i2}$ from the current $\underline{I}_{i1}$ in the *i*-th phase) and the angle $\varphi_2$ ( $\varphi_2$ is the phase angle between the current $\underline{I}_{i1}$ in the *i*-th phase of the first line and the resulting current obtained by subtracting the current $\underline{I}_{i1}$ from the current $\underline{I}_{i2}$ ). The condition for the protection trip to disable the damaged line is the following inequalities (1, 3, 5 - to disable the first line, 1, 2, 4 - to disable the second one):

$$\left(I_{i1}-I_{i2}\right)\geq k_1\left(I_{i1}+I_{i2}\right); \quad (1)$$

$$\varphi_1-\varphi_2>0; \quad (2)$$

$$\varphi_1-\varphi_2<0; \quad (3)$$

$$I_{i1}\geq k_2 I_{idl1}; \quad (4)$$

$$I_{i2}\geq k_2 I_{idl2}, \quad (5)$$

where $I_{i1}$ and $I_{i2}$ are the absolute currents values in the i-th phase of the first and second lines; $k_1$, $k_2$ - tuning out coefficients; $I_{idl1}$, $I_{idl2}$ - idle currents of the first and second lines; $\varphi_1=\left(\underline{I}_{i2}-\underline{I}_{i1}\right)^\wedge \underline{I}_{i1}$; $\varphi_2=\left(\underline{I}_{i1}-\underline{I}_{i2}\right)^\wedge \underline{I}_{i2}$.

In the load mode, in the absence of short circuits on the protected lines, all line phases have currents. At the same time, signals proportional to the measured currents appear at the current sensors 1, 2 outputs (Fig. 4), but with different values due to errors of the sensors themselves. Therefore, units 3, 4 of the presence of currents in the line phases control (control the fulfillment of inequations (4), (5)), units 5, 6 of the angles $\varphi_1$ calculation and $\varphi_2$, subtractor 7, comparison unit 8 (if $\varphi_1>\varphi_2$) and unit 9, calculating the ratio of the difference between the currents of the same name phases to their sum, send signals. The comparison unit 10 does not send a signal, since (1) has not been completed. As a result, there are no signals at the outputs of the AND elements 11, 12, and the protection does not work.

During short circuit, for example, on the first line between phases A and B, currents are present in both lines. Therefore, units 3, 4 give signals. Since the short circuit is in the first line, the currents in its phases A and B are higher than the currents in the same phases of the second line. Therefore, (1) is executed and the comparison unit 10 gives a signal to the input of the AND elements 11, 12. In this case, the comparison circuit 8 does not produce a signal, since (3) is executed, as illustrated in Fig. 5a. Therefore, from the AND element 12 output the signal enters the first line breaker disconnect circuit.

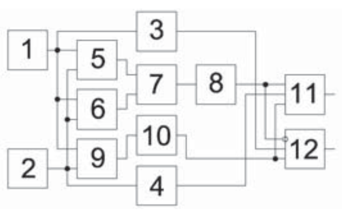


Fig. 4. The block diagram of the parallel lines protection from the supply side, controlling the currents difference in the same name phases vector angle

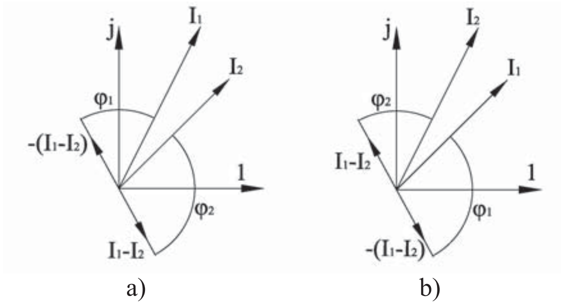


Fig. 5. The phase shift angles between the difference of currents in the same phases and currents in phases: a - with short circuit in the first line; b - with short circuit in the second line

During short circuit, for example, on the second line between phases A and B in the cascade zone, after the circuit breaker at the receiving side of the second line is disconnected, there is no current in its phase C, but is present in phase C of the first line. Therefore, (1) is executed, but (5) is not, and the protection for disconnecting the first line does not work. In this case, currents in phases A and B of both lines are present, and currents in the second line exceed the currents in the first one (Fig. 5b). Therefore, (1) is executed, and the comparison unit 10 gives a signal to the inputs of the AND elements 11, 12; (2) is executed, and the comparison unit 8 gives a signal; (4) and (5) are executed, and units 3, 4 give signals to the inputs of AND elements 11, 12. As a result, at the output of the AND element 11, a signal appears indicating the presence of damage on the second line, and the protection trips to disconnect its switch on the supply side. Similarly, the protection operation in other modes is analyzed.

## III. Method for Protecting Parallel Lines at the Consumer Side

The protection principle [32] is to control the time between the moments when the current $i$ in the line phase reaches the set value in the positive (negative) half-wave. The line for which the measured time is less than $t_{ref1}=0.015$ s or exceeds $t_{ref2}=0.025$ s is disconnected. In load mode from the outputs of current sensors 1 currents in the line phases are sent to the inputs of units 3, 4. When signals $i_1$ and $i_2$ reach the value $i_{ref}$ for the first time at the current rise in the positive half-wave, units 3, 4 trip and start the countdown in units 5, 6 (they measure the time $t_1$ and $t_2$ between the moments when $i_1=i_{ref}$ and $i_2=i_{ref}$ during the current rise to the positive half-wave), and in blocks 7, 8 when the current rises to the negative half-wave (they measure the time $t_3$ and $t_4$ between the moments when $i_1=i_{ref}$ and $i_2=i_{ref}$ during the current rise in the negative half-wave). When signals $i_1$ and $i_2$ reach the value $i_{ref}$ for the second time, the first countdown stops, and units 5 and 6 send signals to the inputs of units 9, 10 and 11, 12, respectively (compare each of $t_1$ and $t_2$ with $t_{ref1}$ and $t_{ref2}$), and units 7 and 8 - to the inputs of units 13, 14 and 15, 16 (compare each of $t_3$ and $t_4$ with $t_{ref1}$ and $t_{ref2}$), and the next time count starts. At the same time, units 9 and 11 do not send signals, since $t_1 \geq t_{ref1}$ and $t_2 \geq t_{ref1}$, units 10 and 12 - since $t_1 \leq t_{ref2}$ and $t_2 \leq t_{ref2}$, units 13 and 15 - since $t_3 \geq t_{ref1}$ and $t_4 \geq t_{ref1}$, units 14 and 16 - since $t_3 \leq t_{ref2}$ and $t_4 \leq t_{ref2}$. Therefore, there are no signals at the outputs of OR elements 17, 18 and executive elements 19, 20, and the protection does not work.

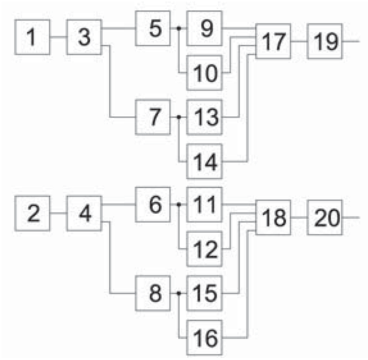


Fig. 6. Block diagram of the parallel lines protection installed at consumer side

Consider a short circuit, for example, on the first line when the currents decrease to a negative half-wave at the moment when $i_1 > i_{ref}$ (Fig. 7). Until short-circuit occurs, the signals are fed from the outputs of units 3, 4, to the inputs of units 5, 7 and 6, 8, which begin to count the corresponding time. After the short circuit occurs, when $i_1 = i_{ref}$ during the current rise, units 3, 4 send signals, stopping the countdown in units 5, 6. From the outputs of the latter, the signals are sent to the inputs of the comparison units 9, 10 and 11, 12. Moreover, since the current in the first line switched the phase to the opposite, the time $t_1$, measured by unit 5 exceeds $t_{ref2}$. Therefore, unit 10 sends a signal through an OR element 17 to the input of the execute element 19, which sends a signal to disconnect the first line switch. Similarly, the protection operation in other modes is analyzed.

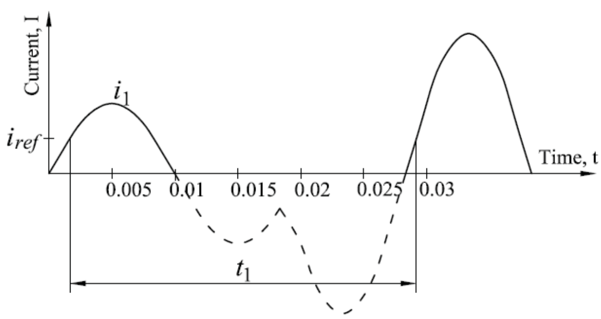


Fig. 7. The time between the moments when the current reaches the the set value in the line phase when it rises during a short circuit

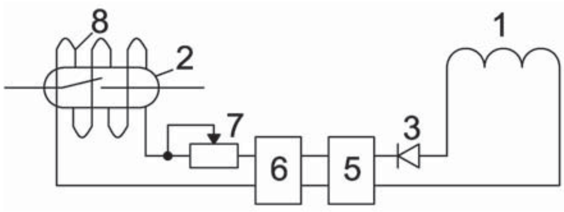


Fig. 8. Schematic diagram of the reed switch trip polarity provision

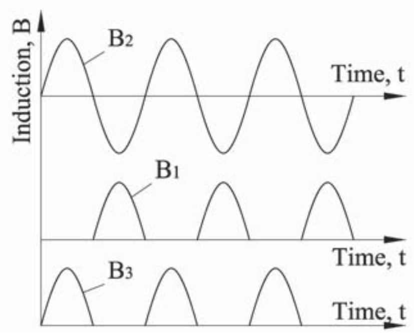


Fig. 9. Schematic diagram of the reed switch trip polarity provision

If the above current sensors are made with the reed switches, their response polarity can be ensured in accordance with the circuit [33] shown in Fig. 8. When current flows in the conductor at the terminals of the induction coil 1 installed like the reed switch 2, near this conductor, the EMF variable is induced. With diode 3, a half-wave of this EMF is distinguished: a positive one - if it is necessary that the reed switch 2 is triggered during a positive half-wave of current in the conductor; a negative one - if it is necessary during a negative one. The allocated EMF half-wave is increased by an amplifier 5, shifts in phase using a phase-shifting circuit 6, and fed through an adjustable resistor 7 to a control winding 8 installed on a reed switch 4. The amplifier 5 increases the indicated half-wave of the EMF variable, and the phase-shifting circuit shifts it in phase so that a current flows through the control winding 8, creating a magnetic field with induction $B_1$ (Fig. 9) equal to the induction $B_2$ of the magnetic field created by the current in bus 1, but shifted in phase by $180^0$. Therefore, the resulting magnetic field with induction $B_3$ affects the reed switch 2.

## IV. CONCLUSIONS

The proposed three methods allow to construct the parallel line protection in networks with an insulated neutral both from the supply and from the receiving side without current and voltage transformers. At the same time, as the above analysis showed, the devices that implement them will work correctly in all modes, and have the following important advantages over protections in operation: they are not tuned out from currents in intact phases and from maximum load currents.

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