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Improving the Reliability of Diagnosing Reed Switch-Based Overcurrent Protection Circuits

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***Abstract*—This paper analyzes known circuitries of reed switch-based overcurrent protections. Notably, diagnostics-incapable circuitries tend to be unreliable as they issue false positives when reed switch contacts are stuck or when an element of the circuitry fails. Integrity diagnostics-featuring circuitries are not unflawed either. One is only able to diagnose its reed switch, the other one diagnoses everything but the reed switch, and the third one only features test diagnostics. Besides, the first two on the list may issue false positives when the diagnostic circuit is faulty. To improve the reliability of diagnosing reed switch-based overcurrent protections, the authors hereof developed a circuitry that checks the integrity of reed switches, protections, and its elements alike. The viability of this new design has been tested by thought experiments and computer simulations in Multisim 14.**

Keywords—overcurrent protection; reed switch; integrity check; Multisim

I. Introduction

Current transformers are inherently flawed [1-3][4-7], making the development of transformer-free protections a relevant undertaking. One solution lies in using reed switch-based protections [2, 8]. Several principles [10-14] and protections [15-19] using reed switches have already been proposed. Most of the papers [20-26] dwell upon overcurrent protections as these are among the simplest and most common protections used in 3 kV to 110 kV grids [27-29]. The simplest circuitry [20] contains a reed switch mounted at a safe distance (per safety guidelines) from the conductive busbars, with a pulse expander connected to its contacts and an actuator connected to the expander. The circuitries in [21] have similarly mounted reed switches that are connected to a microprocessor, which calculates the current in the conductor. The circuitries in [22, 23] have their reed switches contained in an insulated enclosure mounted directly upon the busbars with the protection unit being connected to the contacts of the switch. However, these designs are unreliable as they can issue a false positive if the contacts of the reed switch are stuck or if some elements of the circuits fail.

Studies [24-26] attempted to improve the reliability of reed switch-based overcurrent protections. The one presented in [24] only checks if the reed switch contacts are stuck, the one in [25] features test diagnostics of the entire protection system, and the one in [26] runs self-diagnostics of the protection logics and actuation without checking the reed switch. Besides, the protections presented in [24, 26] can issue incorrect actions if the diagnostic circuit is faulty. This is why this paper proposes a protection that has the advantages of [24, 26] while capable of self-diagnosing reed switches and the elements of the diagnostic circuit alike.

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II. Overcurrent Protection Circuit Featuring Functional Integrity Diagnostics

Figure 1 shows the reed switches (1) and (2) with their spade terminals (5, 6, 9) and (7, 8, 10). The reed switches are to be placed near a phase in the electric facility to be protected; the timers (3, 4, 13, 14, 22, 23, 30, 35, 36, 49, 56 to 60); the logical elements AND (11, 42), OR (15, 17, 18, 19, 20, 37), AND (21) with a single inverse input, AND (39) with two inverse inputs, AND-NOT (40), NOT (61); the slow-release relays (16, 38, 53, 54, 55); the memory units (12, 34, 50); the protection unit (28); the clock generators, CG (43, 48); the control windings (44, 51); the button (41); the intermediate relays (26, 27) with the opening contacts (24 and 32, 25 and 33) and those with the closing contacts (46, 47); the relay (29) with the closing contacts (31, 52). For the timers and the memory units, S stands for the "start" input, R stands for "reset". The CGs (43, 48) issue pulses at 100 Hz lasting 0.004 to 0.0095 s according to how long reed switch contacts are closed.

Let us analyze how this circuitry works by thought experiment, which is deemed [30] a modeling method that provides a logical analogy to real-world experimentation. When the protection is on, and there is no short circuit in the protected electric facility, the magnetic induction produced by the current running in the busbar of that facility will not be enough to trigger the reed switches 1 and 2. Thus, the spade terminals (5 and 6, 7 and 8) will remain open, with the OR elements (15, 37) not issuing any signals. Once the protection has been initiated, its runs functional diagnostics to check the protection integrity; this is done by pressing the self-locking button (41). As a result, the direct input of the AND element (39) and the "start" inputs of the timers (56 to 60) receive a signal. These timers start counting time and will not issue any signals for a while. The timer (56) is set to equal the delay of the slow-release relay (53), e.g. 300 s. It signals if the relay (53) and the OR element (17) are faulty. The timer (57) is set to equal the delay of the slow-release relay (54), e.g. 5 s. It

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signals if the relay (54) and the OR element (18) are faulty. The timer (58) is set to equal the delay of the slow-release relay (55), e.g. 3 s. It signals if the relay (55) and the OR element (19) are faulty. If the timers (56 to 58) are set for a shorter time, they will false-positively signal their elements faulty. The timers (59, 60) are set e.g. to 301 s to be slightly longer than the time between the intervals separating the protection integrity checks e.g. 300 s. These timers signal if the reed switches (1, 2) are faulty whether in diagnostic mode or in SC mode, hence the setting. The time (e.g. 300 s) between self-diagnostic runs is configured to provide the necessary lifespan of a reed switch, or to 15 hours as in [31]. The output of the AND element (39) produces a signal as its inverse inputs do not receive signals from the OR elements (19, 37). This signal goes to the input of the OR-NOT element (40) and to the inverse input of the AND element (21), blocking them; it also goes to the inputs

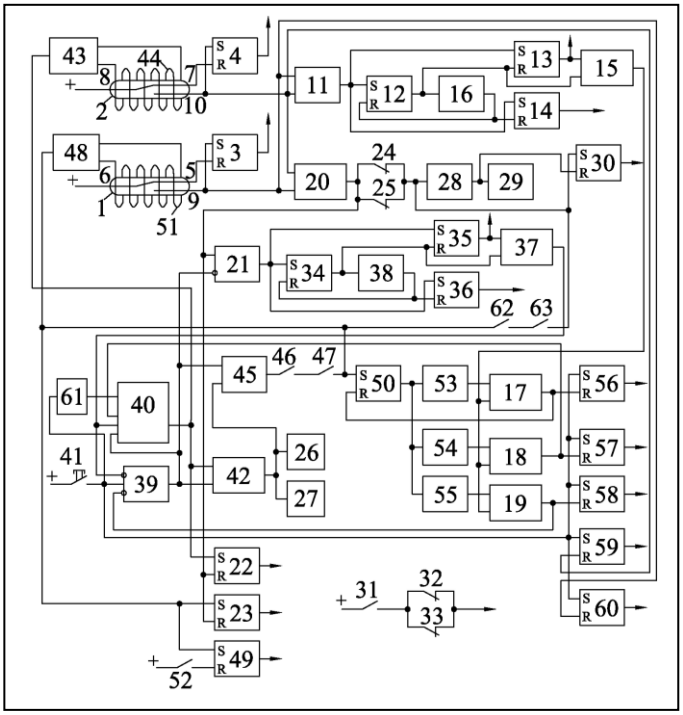

Fig. 1. Reed switch-based protection with functional diagnostics: circuit diagram

of the OR element (42) and the AND element (45). The OR element (43) is triggered and issues a signal to the control winding of the intermediate relays (26, 27) as well as to the input of the AND element (45). If the intermediate relays (26, 27) are intact, they open the normally closed contacts (24, 32 and 25, 33) and close the normally open contacts (46, 62 and 47, 63), also triggering the AND element (45). From the output of the AND element (45), the signal goes through the closed contacts (46, 47, 62, 63) to the "record" input of the memory unit (50), to the "start" inputs of the timers (23, 30, 49), and to the inputs of the protection unit (28) and the clock generator (48), starting them all. The timer (23) signals the faults of: the clock generator (48), the control winding (51), the reed switch (1), and the OR element (20); for this reason, it has a delay (e.g. 0.02 s) necessary for the signal to go from the AND element (45) to the control winding (51) so that the reed switch (1) could be triggered. The timer (30) signals the fault of the protection unit (28), which is why its delay should be sufficient for the unit to respond. The timer (49) signals the fault of the intermediate relay (29) and therefore is set to a time sufficient for the protection unit (28) to respond and for the relay to actuate. If the timers (23, 30, 49) are set to a shorter countdown, their "reset" inputs will receive a signal after the timers go off, signaling the corresponding elements faulty, which is unacceptable. The memory unit (50) stores the received signal and issues it to the inputs of the slow-release relays (53 to 55) until receiving a "reset" input. The slow-release relays (53 to 55) start their countdown. The relay (53) restarts the diagnostic procedure after a set time, e.g. 300 s. The slow-release relay (55) issues a signal to the input of the protection unit (28) over a time (e.g. 3 s) said unit needs to respond and the intermediate relay (29) needs to actuate; it also controls the duration of the integrity check for the reed switch (1). The relay (54) has a longer delay than (55), e.g. 5 s, and controls the duration of the integrity check for the reed switch (2). The relay (54) needs such a delay because the reed switch (2) is only subject to checking once its counterpart (1) has been checked. This enables the detection of short circuits in the protected facility while running the integrity check. A signal clocked to 0.01 s, lasting 0.0095 s at max is produced by the clock generator (48) and goes to the control winding (51). The reed switch (1) begins closing the spade terminals (6 and 9), starting the timer (3), or closing the terminals (5 and 6), resetting the timer (3), alternating between the two operations. The timer (3) is set e.g. to 0.02 s to check if the contacts of the reed switch (1) are stuck. If the reed switch (1) is intact, starting the timer (3) also resets the timer (60) and, through the OR element (20), the timer (23). After the delay time expires, the intact protection unit (28) will issue a signal to the control winding of the intermediate relay (29) and to the "reset" input of the timer (30), stopping the countdown. If the relay (29) is intact, its normally open contacts (31, 52) will close. This will stop the timer (49), and no signal will go to the tripping circuit of the circuit breaker, since the normally closed contacts (32, 33) of the intermediate relays (26, 27) are open. After the delay expires, the slow-release relay (55) will issue a signal to the input of the OR element (19), which will further send the signal to the inverse input of the AND element (39), blocking it. As a result, the clock generator (48) stops issuing its signal, the reed switch (1) returns to its initial state. However, the OR element (42) keeps signaling as it has received an input from the OR-NOT element (40), which is not receiving inputs from the OR elements (18, 37), the AND element (39), or the NOT element (61). This effectively starts the timer (22) and the clock generator (43), which issues a signal to the control winding (44) of the reed switch (2). The timer (22) begins a countdown (same as the timer's (23)), and the reed switch (2) begins closing the spade terminals (8, 10) to start the timer (4), which has the same delay as the timer (3), or closing the spade terminals (8, 7), resetting the timer (4); it alternates between the two operations. If the reed switch (1) is intact, starting the timer (4) also resets the timer (59) and, through the OR element (20), the timer (22). After the delay expires, the slow-release relay (54) will issue a signal to the input of the OR element (18), which will further send the signal to inverse input of the OR-NOT element (40), blocking

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it. This returns the clock generator (43), the reed switch (2), the AND element (45), and the intermediate relays (26, 27) to their respective initial states, whereby the relays do so with a delay, e.g. 0.1 s. The protection unit (28) stops receiving input, thus also resetting to the initial state. After the configured delay of e.g. 300 s expires, the slow-release relay (53) signals "reset" to the memory unit (50) via the OR element (17). This causes the slow-release relays (53 to 55) and the OR elements (17 to 19) to stop signaling; the AND element (39) receives an input. Protection integrity diagnostic is run again.

If while integrity check is in process, the protected facility short-circuits, e.g. while the reed switch (1) is being triggered, the current surge in the busbar will trigger the reed switch (2). This causes the AND element (11) to issue an output, activating the memory unit (12) and the timers (13, 14). The timer (14) has a delay of e.g. 0.01 s as necessary to trigger the memory unit (12), as this timer signals that unit's fault. If the memory unit (12) issues an output, the timer (13) stops its countdown (e.g. 0.01 s), the slow-release relay (16) begins its, and the OR element (15) issues a signal. The slow-release relay (16) has a delay long enough for the protection unit (28) to respond and for the intermediate relay (29) to actuate, tripping the circuit breaker, and resetting the intermediate relays (26, 27). This is necessary for eliminating the short circuit in the protected facility. The timer (14) has the same delay as it signals faults in the slow-release relay (16). The OR element (15) issues a signal to the OR elements (17 to 19), the output signals of which block the AND element (39), the OR-NOT element (40), the memory unit (50), and the timers (56 to 58). This stops the integrity check. In that case, the protection unit (28) triggered during the procedure will return to the initial state while the contacts (24, 25) are being closed (the intermediate relays (26, 27) have a return delay, e.g. 0.1 s). This is necessary for overcurrent protection not to become a quick-response protection, and for the current cutoff not to lose its interference-proof quality. Therefore, when the OR element (20) produces an output signal after the reed switches (1, 2) have been triggered, the protection unit (28) will be activated again and deliver a signal to the input of the intermediate relay (28) after a delay. This relay will close the normally open contacts (31, 52), issuing a signal to the circuit-breaker tripping circuit and stopping the countdown of the timer (49). The protection will have effect. Once the circuit breaker has been tripped, the integrity check continues.

If between the integrity checks, an SC occurs, or e.g. the reed switch (1) fails to respond, the reed switch (2) will, sending a signal through the OR element (20) to the direct input of the AND element (21). Since the diagnostic procedure (a check) has not started, the AND element (39) is producing no output signal; this causes the AND element (21) to issue a signal, activating the memory unit (34) and the timers (35, 36). The timers (35, 36) have the same delays as the timers (13, 14), respectively. The memory unit (34) issues a signal and starts the countdown (same as in the relay (16)) in the slow-release relay (38), stops the countdown in the timer (35), and triggers the OR element (37), whose signal will block the AND element (39) and the OR-NOT element (40). After a delay, the slow-release relay (38) will reset the memory unit (34) and initiate the protection integrity check. In this case, the signal from the reed switch (2) will go through the OR element (21) and the normally closed contacts (24, 25) of the intermediate relays (26, 27) to the protection unit (28), activating it. The protection will have effect, the intermediate relay (29) will close the contacts (31) and signal to the tripping circuit of the circuit breaker.

If any of the described elements fails and does not issue a signal, the corresponding timer will finish the countdown as it does not receive a "reset" input, therefore signaling a fault in the circuit. For instance, if the reed switches (1, 2) fail to respond when starting the next diagnostic cycle, the timers (59, 60) will go off; if they fail to respond during a diagnostic procedure, the timers (22, 23) will. If the spade terminals (5, 6 or 7, 8) are stuck, the timers (3) or (4) will go off. The integrity of all other elements is monitored in the same fashion.

In case the protection unit (28) uses a current cutoff, it will only be triggered when the reed switches (1) and (2) are triggered for the third time. Besides, the unit (28) has a protection and alarm lock in case the contacts of the reed switches (1, 2) are stuck; the timers (3, 4) are merely a redundancy. Notably, the proposed protection can identify faults in some of the elements of the diagnostic circuit. Besides, like some cutting-edge microprocessor-based protections e.g. Toshiba's GRD 140, it diagnoses all of its elements including the relay input and the output that trips the circuit breaker.

Special mounts [32] can be used to mount reed switches or the whole protection system near busbars; these mounts allow adjusting the reed switch position in space.

III. Multisim 14 Simulations

Figure 2 shows the simulated protection circuitry with some element groups being merged into blocks. Positional numbers in Figure 2 match those in Figure 1. Block-merged elements are: (90) for the reed switches (1, 2) with induction coils (44, 51) and the clock generators (43, 48); (91) for the AND element (11), the OR element (15), the memory unit (12), the timers (13, 14), and the slow-release relay (16); (92) for the OR elements (20, 37), the AND element (21) featuring inverse inputs, the memory unit (34), the timers (35, 36), and the slow-release relay (38); (93) for the OR-NOT element (40), the OR element (42), and the NOT element (61); (94) for the intermediate relay (26) with the contacts (24, 32, 46, 62), the intermediate relay (27) with the contacts (25, 33, 47, 63), and the AND element (45); (95) for the OR elements (17 to 19) and the slow-release relays (53 to 55).

To implement some of the functions, the research team added some extra elements, resulting in some minor changes in the connection diagram. Block (96) was added to ensure that the contacts (24, 25) of the intermediate relays (26, 27) be closed with a delay. In the block (92), the inverse input of the AND element (21) is implemented by using a NOT element whose output goes to the direct input of the AND element (21). Keys (85 to 89) are designed to simulate a failure in a circuit element, whereas the keys (87, 88) simulate a short circuit. The resistors (64 to 84) are needed for correct circuitry testing in the software; they will also be needed when

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assembling the actual circuitry. The clock generator (99) imitates the magnetic field of the busbar current as affected by a short circuit. Light (108) signals that the protection has been triggered; the lights (100 to 107, 109 to 115) signal a detected fault. The reed switches (1, 2) and the induction coils (44, 51) the carry are implemented using two controllable keys; the memory units are based on RS triggers.

Figure 3 shows an example of connecting the elements merged in the blocks (90) and (93). Other blocks are not shown as they could be easily modeled by analogy. A fully assembled circuitry has been tested in a variety of operation conditions; the testing proved the proposed system viable.

IV. Conclusions

This paper proposes a reed switch-based overcurrent protection circuitry that features functional integrity checks and does not use current transformers. Unlike its counterparts, this new circuitry monitors the integrity of the reed switch, the protection, and the diagnostic circuit elements alike. The design has been proven viable by thought experiments and simulations in Multisim 14.

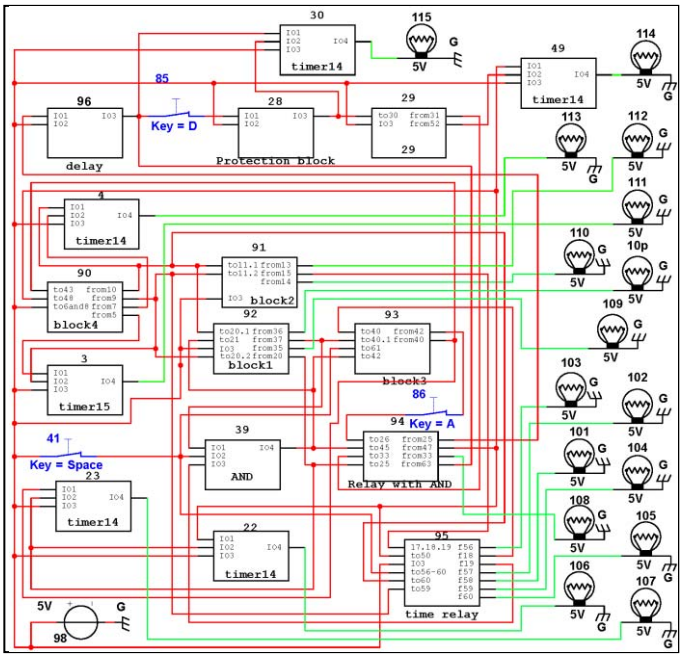

Fig. 2. Overcurrent protection with self-diagnostics: a Multisim model

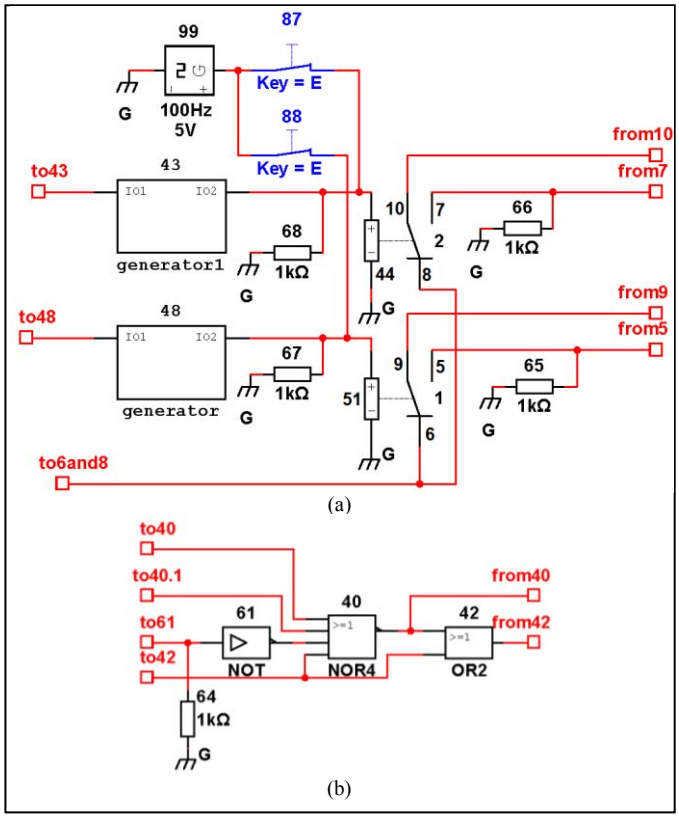

Fig. 3. Elements in blocks (90) and (93): connection circuit

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